# PIP212-12M

## DC-to-DC converter powertrain

Rev. 04 — 23 October 2006 Product data sheet

## 1. General description

The PIP212-12M is a fully optimized powertrain for high current high frequency synchronous buck DC-to-DC applications. The PIP212-12M replaces two power MOSFETs, a Schottky diode and a driver IC, resulting in a significant increase in power density. The integrated solution allows for optimization of individual components and greatly reduces the parasitics associated with conventional discrete solutions, resulting in higher system efficiencies at higher frequency operation.

## 2. Features

- Input conversion ranges from 3.3 V to 16 V
- Output voltages from 0.8 V to 6 V
- Capable of up to 35 A maximum output current at 1 MHz
- Operating frequency up to 1 MHz
- Peak system efficiency > 90 % at 500 MHz
- Automatic Dead-time Reduction (ADR) for maximum efficiency
- Internal thermal shutdown
- Auxiliary 5 V output
- Power ready output flag
- Power sequencing functions
- Internal 6.5 V regulator for efficient gate drive
- Compatible for single and multi-phase Pulse Width Modulation (PWM) controllers
- Low-profile, surface-mounted package (8 mm $\times$ 8 mm $\times$ 0.85 mm)

## 3. Applications

- High-current DC-to-DC point-of-load converters
- Small form-factor voltage regulator modules
- Microprocessor and memory voltage regulators
- Intel DriverMOS (DrMOS) compatible

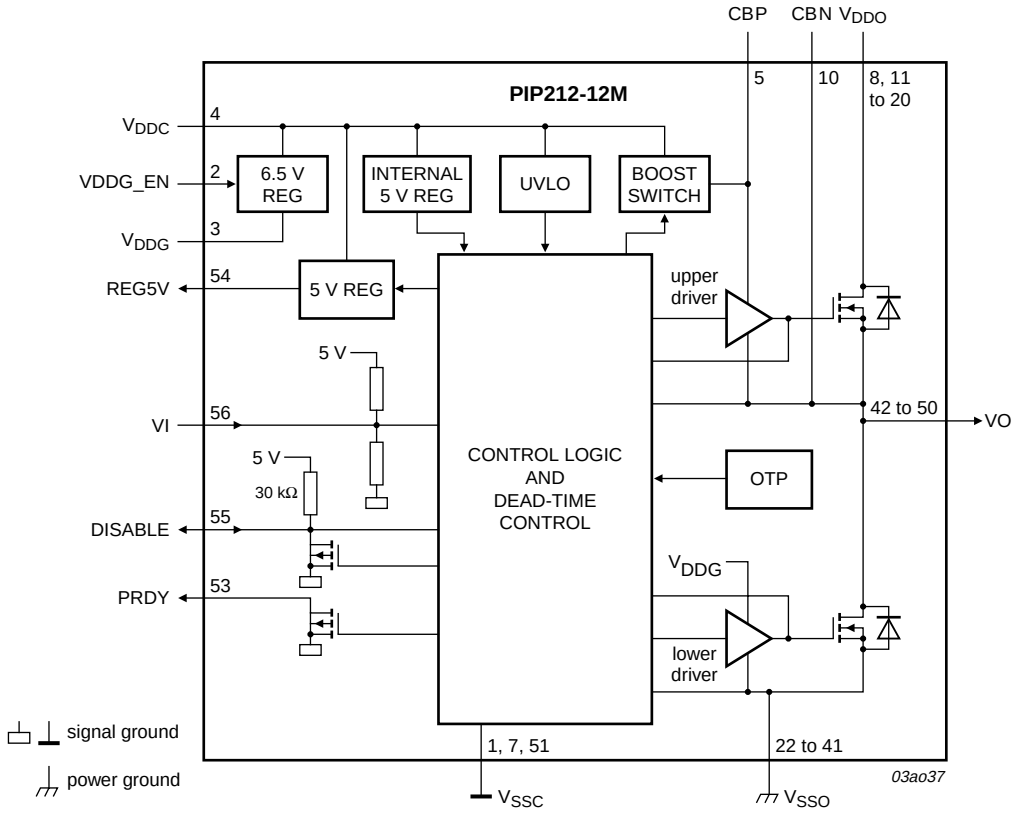
NXP founded by Philips

# 4. Ordering information

**Table 1. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| PIP212-12M | HVQFN56 | plastic thermal enhanced very thin quad flat package; no leads; 56 terminals; body 8 × 8 × 0.85 mm | SOT684-4 |

# 5. Block diagram




A bootstrap switch is integrated into the design of the PIP212-12M between $V_{DDC}$ and CBN

**Fig 1. Block diagram**



© NXP B.V. 2006. All rights reserved.

# 6. Functional diagram

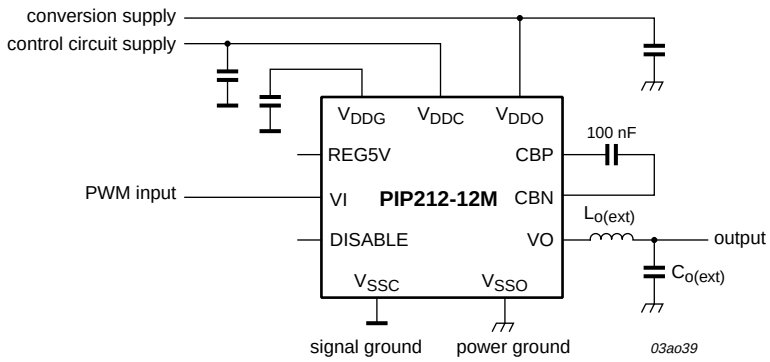



**Fig 2. Simplified functional block diagram of a synchronous DC-to-DC converter output stage**

# 7. Pinning information

## 7.1 Pinning

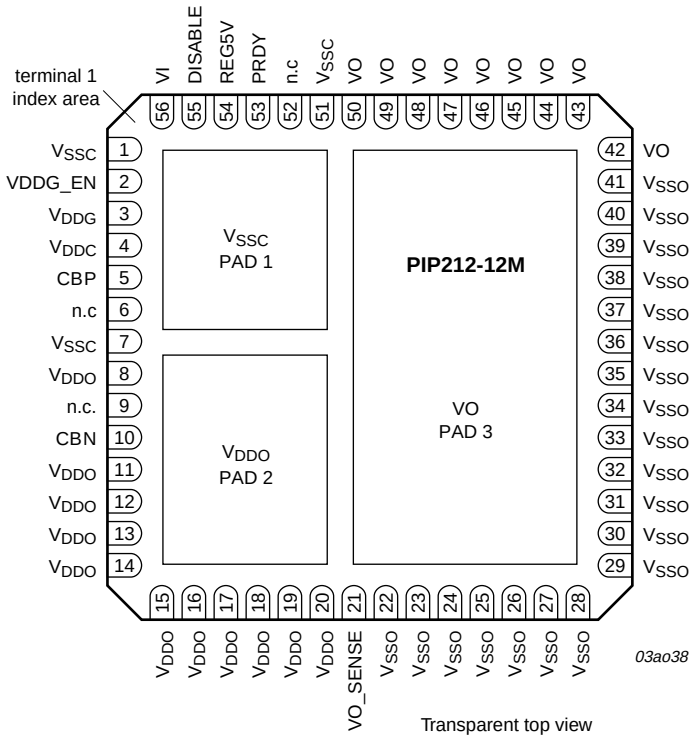



**Fig 3. Pin configuration**



© NXP B.V. 2006. All rights reserved.

### 7.2 Pin description

Table 2. Pin description

| Symbol | Pin | Type | Description |
|---|---|---|---|
| $V_{DDC}$ | 4 | - | control circuit supply voltage |
| $V_{DDO}$ | 8, 11 to 20, pad 2 | I | output stage supply voltage |
| $V_{SSC}$ | 1, 7, 51, pad 1 | - | control circuit ground |
| $V_{SSO}$ | 22 to 41 | - | output stage ground supply voltage |
| VI | 56 | I | pulse width modulated input |
| VO | 42 to 50, pad 3 | O | output voltage |
| VO_SENSE | 21 | O | sense connection to VO often required by PWM for current sensing |
| CBP | 5 | - | connection to bootstrap capacitor |
| CBN | 10 | - | connection to bootstrap capacitor |
| VDDG_EN | 2 | I | enables internal 6.5 V regulator for $V_{DDG}$ |
| $V_{DDG}$ | 3 | - | gate driver supply voltage |
| PRDY | 53 | O | indicates that $V_{DDC}$ is above the UVLO (UnderVoltage Lockout) level (open drain) |
| REG5V | 54 | O | 5 V regulated supply output |
| DISABLE | 55 | I/O | disable driver function (active LOW) |
| n.c. | 6, 9, 52 | - | not connected - leave open or connected to GND on PCB (Printed-Circuit Board) layout |

## 8. Functional description

### 8.1 Basic operation

The PIP212-12M combines two MOSFET transistors and a MOSFET driver in a thermally enhanced low inductance package for use in high frequency and high efficiency synchronous buck DC-to-DC converters; see Figure 2. The two MOSFETs are connected in a half bridge configuration between $V_{DDO}$ and $V_{SSO}$. The mid point of the two transistors is $V_O$ which is connected to the output of a DC-to-DC converter via an inductor. A logic HIGH signal on the VI pin causes the lower MOSFET to be switched off and the upper MOSFET to be switched on. Current will then flow from the supply ($V_{DDO}$), through the upper MOSFET and the inductor ($L_{o(ext)}$) to the output.

A logic LOW signal on the VI pin causes the upper MOSFET to be turned off and the lower MOSFET to be switched on. Current then flows from the power ground ($V_{SSO}$), through the lower MOSFET and the inductor ($L_{o(ext)}$), to the output. The output voltage is determined by the ratio of time that the upper and lower MOSFETs conduct.

### 8.2 UnderVoltage Lockout (UVLO)

The UVLO function ensures the correct operation of the control circuit during a power-up and power-down sequence. Power to the control circuit is provided by the $V_{DDC}$ pin. This voltage is internally monitored to ensure that if $V_{DDC}$ is below the UVLO threshold, the DISABLE pin is internally pulled LOW and both MOSFETs are off. This is indicated by the power ready (PRDY) flag, an open drain output that is pulled LOW whenever $V_{DDC}$ is below the UVLO threshold.


© NXP B.V. 2006. All rights reserved.

## 8.3 Upper driver operation

The gate drive to the upper MOSFET is provided by a bootstrap capacitor (typically 100 nF) that is placed between the CBP and CBN pins. This capacitor is charged via an internal boost switch to a voltage within a few millivolts of $V_{DDC}$ up to a maximum of 12 V (this is to prevent excessive gate charge losses when $V_{DDC}$ > 12 V). The upper MOSFET will be switched according to PWM input once the boost capacitor voltage is above $V_{th(CBP-CBN)}$ on. When ever the voltage is below $V_{th(CBP-CBN)}$ off the upper MOSFET will remain off.

## 8.4 $V_{DDG}$ regulator

The gate drive to the lower MOSFET is provided by the $V_{DDG}$ pin. A 1 µF capacitor should be connected between this pin and $V_{SSC}$. For minimum power loss within the PIP212-12M, an external power supply of between 5 V and 12 V should be connected to this pin. The optimum value for this voltage is dependent on the application but in the majority of cases a 5 V supply is recommended; see Figure 11. In cases where the $V_{DDG}$ maximum voltage will not be exceeded, the $V_{DDG}$ pin can be connected to the $V_{DDC}$ pin and the $V_{DDG}$ capacitor can be omitted; see Figure 13.

When $V_{DDC}$ is connected to a supply greater than 9 V, an internal 6.5 V regulator connected to $V_{DDG}$ can be used to provide the gate drive for the lower MOSFET; see Figure 12. The $V_{DDG}$ regulator is enabled by leaving the VDDG_EN pin open resulting in this pin being pulled internally to 5 V. If an external supply is to be connected to $V_{DDG}$ then the VDDG_EN pin must be connected to $V_{SSC}$ to disable the internal $V_{DDG}$ regulator.

**Table 3. $V_{DDG}$ biasing**

| VDDG_EN | $V_{DDG}$ |
|---|---|
| Open circuit | internal 6.5 V regulator used ($V_{DDC}$ > 9 V) |
| $V_{SSC}$ | connection to external supply required |

## 8.5 3-state function

If the input to VI from the PWM controller becomes high impedance, then the VI input is driven to 2.5 V by an internal voltage divider. A voltage on the VI pin that is in-between the $V_{IH}$ and $V_{IL}$ levels and present for longer than $t_{d(3\text{-state})}$, causes both MOSFETs to be turned off. Normal operation commences once the VI input is outside this window for longer than $t_{d(3\text{-state})}$.

## 8.6 Automatic Dead-time Reduction (ADR)

Protection against cross-conduction (shoot-through) is achieved via the insertion of a delay (or dead-time) between the switching off of one MOSFET and the switching on of the other MOSFET. The automatic dead-time reduction feature continuously monitors the body diode of the lower MOSFET adjusting the dead-time to minimize body diode conduction. This reduces power loss in both the upper and lower MOSFETs due to the reduction in body diode conduction and reverse recovery charge. The lower power dissipation leads to higher system efficiency and enables higher frequency operation.


© NXP B.V. 2006. All rights reserved.

## 8.7 Over Temperature Protection (OTP)

Protection against over temperature is provided by an internal thermal shutdown incorporated into the control circuit. When the control circuit die temperature exceeds the upper thermal trip level, both MOSFETs are switched off and the internal $V_{DDG}$ regulator disabled. This state continues until the die temperature falls below the lower trip temperature. This function is only operational when $V_{DDC}$ is above the UVLO level.

## 8.8 Disable

This is the disable or enable function of the driver. Pulling the DISABLE pin LOW switches off both MOSFETs and disables the REG5V output. This pin is internally pulled LOW whilst $V_{DDC}$ remains below the UVLO threshold. Once $V_{DDC}$ exceeds the UVLO threshold, this pin is pulled HIGH by an internal resistor. In this way the driver will enable itself unless there is an external pull down. In multiphase applications, connecting the DISABLE pins of multiple PIP212-12M devices together will ensure that all devices will only become enabled when the voltage on the $V_{DDC}$ pins of all of the devices has exceeded the UVLO threshold; see Figure 10.

## 8.9 Reg5V

This function provides a low current regulated 5 V output voltage suitable for providing power to a PWM controller. It is operational when both PRDY and DISABLE are HIGH. Operation as a 5 V power supply is only guaranteed when $V_{DDC}$ is > 7 V. This pin can also be used as part of an enable function for a PWM controller; this ensures that the PWM is enabled only when the PIP212-12M is fully operational (i.e. both PRDY and DISABLE are HIGH).



© NXP B.V. 2006. All rights reserved.

# 9. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DDC}$ | control circuit supply voltage | | | –0.5 | +15 | V |
| $V_{DDO}$ | output stage supply voltage | | | –0.5 | +24 | V |
| $V_I$ | input voltage | | | –0.5 | +12.6 | V |
| $V_{DDG}$ | gate driver supply voltage | | | –0.5 | +12.6 | V |
| $V_O$ | output voltage | | | –0.5 | $V_{DDO}$ + 0.5 | V |
| $V_{c(bs)}$ | bootstrap capacitance voltage | | | –0.5 | $V_O$ + 15 | V |
| $I_{O(AV)}$ | average output current | $V_{DDC}$ = 12 V; $T_{pcb} \leq 90$ °C; $f_i$ = 1 MHz | | - | 35 | A |
| $I_{ORM}$ | repetitive peak output current | $V_{DDC}$ = 12 V; $t_p \leq 10$ µs | [1] | - | 60 | A |
| $V_{PRDY}$ | voltage on pin PRDY | | | –0.5 | +12.6 | V |
| $V_{DISABLE}$ | voltage on pin DISABLE | | | –0.5 | +12.6 | V |
| $V_{REG5V}$ | voltage on pin REG5V | | | –0.5 | +12.6 | V |
| $P_{tot}$ | total power dissipation | $T_{mb}$ = 25 °C | [2] | - | 25 | W |
| | | $T_{mb}$ = 90 °C | [2] | - | 12 | W |
| $T_{stg}$ | storage temperature | | | –55 | +150 | °C |
| $T_j$ | junction temperature | | | –55 | +150 | °C |

[1] Pulse width and repetition rate limited by maximum value of $T_j$.

[2] Assumes a thermal resistance from junction to mounting base of 5 K/W.

# 10. Thermal characteristics

**Table 5. Thermal characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{th(j\text{-}mb)}$ | thermal resistance from junction to mounting base | device tested with upper and lower MOSFETs in series | - | 3 | 5 | K/W |



© NXP B.V. 2006. All rights reserved.

# 11. Characteristics

**Table 6: Characteristics**

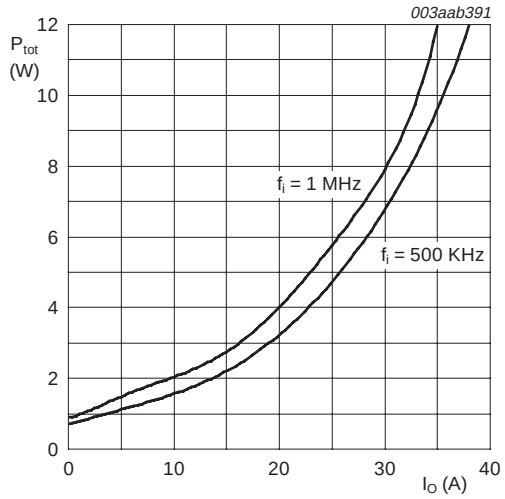
*$V_{DDC}$ = 12 V; $T_j$ = 25 °C unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | | |
| $V_{DDC}$ | control circuit supply voltage | 25 °C ≤ $T_j$ ≤ 150 °C | | 4.5 | 12 | 14 | V |
| $V_{th(UVLO)}$ | undervoltage lockout threshold voltage | turn on | | 4.05 | 4.2 | 4.45 | V |
| | | turn off | | 3.7 | 3.9 | 4.1 | V |
| $V_{th(CBP-CBN)}$ | threshold voltage between pin CBP and pin CBN | turn on | | 3.85 | 4.1 | 4.35 | V |
| | | turn off | | 2.35 | 2.6 | 2.85 | V |
| $V_{IH}$ | HIGH-level input voltage | | [1] | 3.3 | 3.5 | 3.7 | V |
| $V_{IL}$ | LOW-level input voltage | | [1] | 1.4 | 1.5 | 1.6 | V |
| $I_{LI}$ | input leakage current | 0 V ≤ $V_I$ ≤ 5 V | | - | 180 | - | µA |
| $I_{DDC}$ | control circuit supply current | $f_i$ = 0 Hz, $V_I$ = 0 V | | - | 8.4 | - | mA |
| | | $f_i$ = 500 kHz, VDDG_EN = open | | - | 50 | - | mA |
| | | $f_i$ = 500 kHz, VDDG_EN = ground | | - | 12 | - | mA |
| $V_{DDG}$ | gate driver supply voltage | $I_L$ = 65 mA | | 5.75 | 6.5 | 7.25 | V |
| $V_{REG5V}$ | voltage on pin REG5V | $I_L$ ≤ $I_{REG5V}$ minimum, $V_{DDC}$ > 7 V | | 4.5 | 5.0 | 5.5 | V |
| $I_{REG5V}$ | current on pin REG5V | $V_{REG5V}$ = 4.5 V | | 18 | - | - | mA |
| $V_{th(en)}$ | enable threshold voltage | on pin DISABLE, $V_{DDC}$ > 4.5 V | | 2.9 | 3.2 | 3.5 | V |
| $V_{th(dis)}$ | disable threshold voltage | on pin DISABLE, $V_{DDC}$ > 4.5 V | | 1.4 | 1.6 | 1.8 | V |
| $T_{trip(otp)}$ | over-temperature protection trip temperature | | | - | 160 | - | °C |
| $T_{trip(otp)hys}$ | hysteresis of over-temperature protection trip temperature | | | - | 40 | - | °C |
| $P_{tot}$ | total power dissipation | $V_{DDO}$ = 12 V; $I_{O(AV)}$ = 25 A; $V_O$ = 1.3 V; $T_{pcb}$ = 90 °C; | | | | | |
| | | $f_i$ = 500 kHz | | - | 4.5 | - | W |
| | | $f_i$ = 1 MHz | | - | 5.8 | - | W |
| Upper MOSFET | | | | | | | |
| $R_{DSon}$ | drain-source on-state resistance | $I_O$ = 10 A; $V_{CBP}$ = 12 V | | - | 6.5 | - | mΩ |
| Lower MOSFET | | | | | | | |
| $R_{DSon}$ | drain-source on-state resistance | $I_O$ = 10 A; $V_{DDG}$ = 12 V | | - | 1.9 | - | mΩ |
| | | $I_O$ = 10 A; $V_{DDG}$ = 6.5 V | | - | 2.1 | - | mΩ |
| **Dynamic characteristics** | | | | | | | |
| $t_{d(on)(IH-OH)}$ | turn-on delay time from input HIGH to output HIGH | $V_{DDO}$ = 12 V; $I_{O(AV)}$ = 12.5 A | | - | - | 80 | ns |
| $t_{d(off)(IL-OL)}$ | turn-off delay time from input LOW to output LOW | | | - | - | 75 | ns |
| $t_{d(3-state)}$ | 3 state delay time | | | - | 90 | - | ns |

[1] If the input voltage remains between $V_{IH}$ and $V_{IL}$ (2.5 V typ) for longer than $t_{d(3-state)}$, then both MOSFETs are turned off.

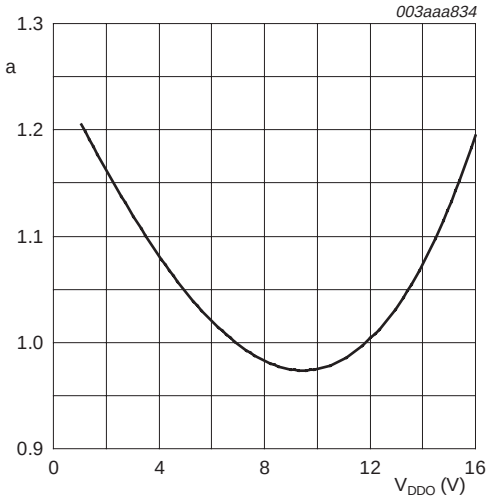


© NXP B.V. 2006. All rights reserved.




$V_{DDC}$ = 12 V; $V_{DDO}$ = 12 V; $V_O$ = 1.3 V; $V_{DDG}$ = 5 V

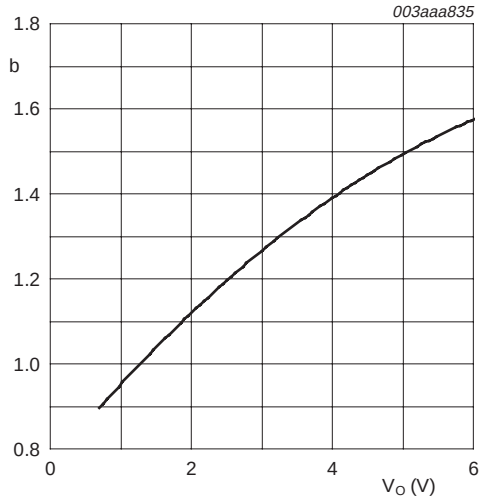
**Fig 4. Total power dissipation as a function of average output current; typical values**




$V_{DDC}$ = 12 V; $V_O$ = 1.3 V; $f_i$ = 1 MHz; $I_{O(AV)}$ = 25 A; $V_{DDG}$ = 5 V

$$a = \frac{P_{tot}}{P_{tot(V_{DDO} = 12\ V)}}$$

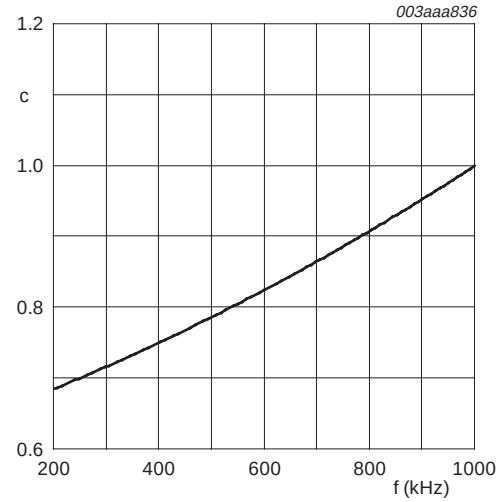
**Fig 5. Normalized power dissipation as a function of output stage supply voltage; typical values**




$V_{DDC}$ = 12 V; $V_{DDO}$ = 12 V; $f_i$ = 1 MHz; $I_{O(AV)}$ = 25 A; $V_{DDG}$ = 5 V

$$b = \frac{P_{tot}}{P_{tot(V_O = 1.3\ V)}}$$

**Fig 6. Normalized power dissipation as a function of output voltage; typical values**



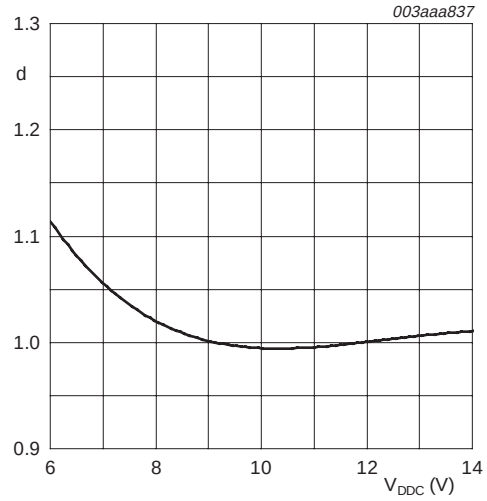

$V_{DDC}$ = 12 V; $V_{DDO}$ = 1.3 V; $V_O$ = 1.3 V; $I_{O(AV)}$ = 25 A; $V_{DDG}$ = 5 V

$$c = \frac{P_{tot}}{P_{tot(f_i = 1\ MHz)}}$$

**Fig 7. Normalized power dissipation as a function of input frequency; typical values**



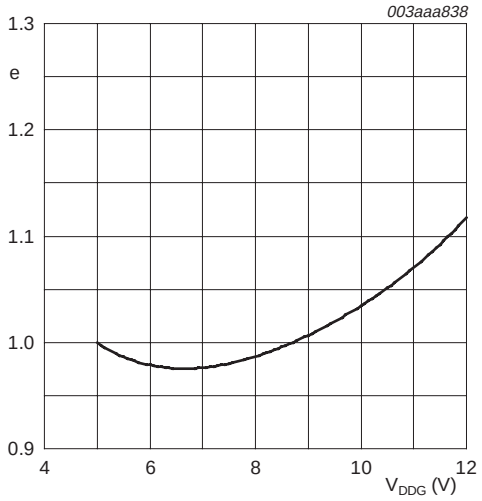
© NXP B.V. 2006. All rights reserved.




$V_{DDO}$ = 12 V; $V_O$ = 1.3 V; $f_i$ = 1 MHz; $I_{O(AV)}$ = 25 A; $V_{DDG}$ = 5 V

$$d = \frac{P_{tot}}{P_{tot(V_{DDC} = 12\,V)}}$$

**Fig 8. Normalized power dissipation as a function of control circuit supply voltage; typical values**




$V_{DDC}$ = 12 V; $V_{DDO}$ = 12 V; $f_i$ = 1 MHz; $I_{O(AV)}$ = 25 A; $V_{DDG}$ = 5 V

$$e = \frac{P_{tot}}{P_{tot(V_{DDG} = 5\,V)}}$$

**Fig 9. Normalized power dissipation as a function of gate driver supply voltage; typical values**



© NXP B.V. 2006. All rights reserved.

# 12. Application information

## 12.1 Typical application

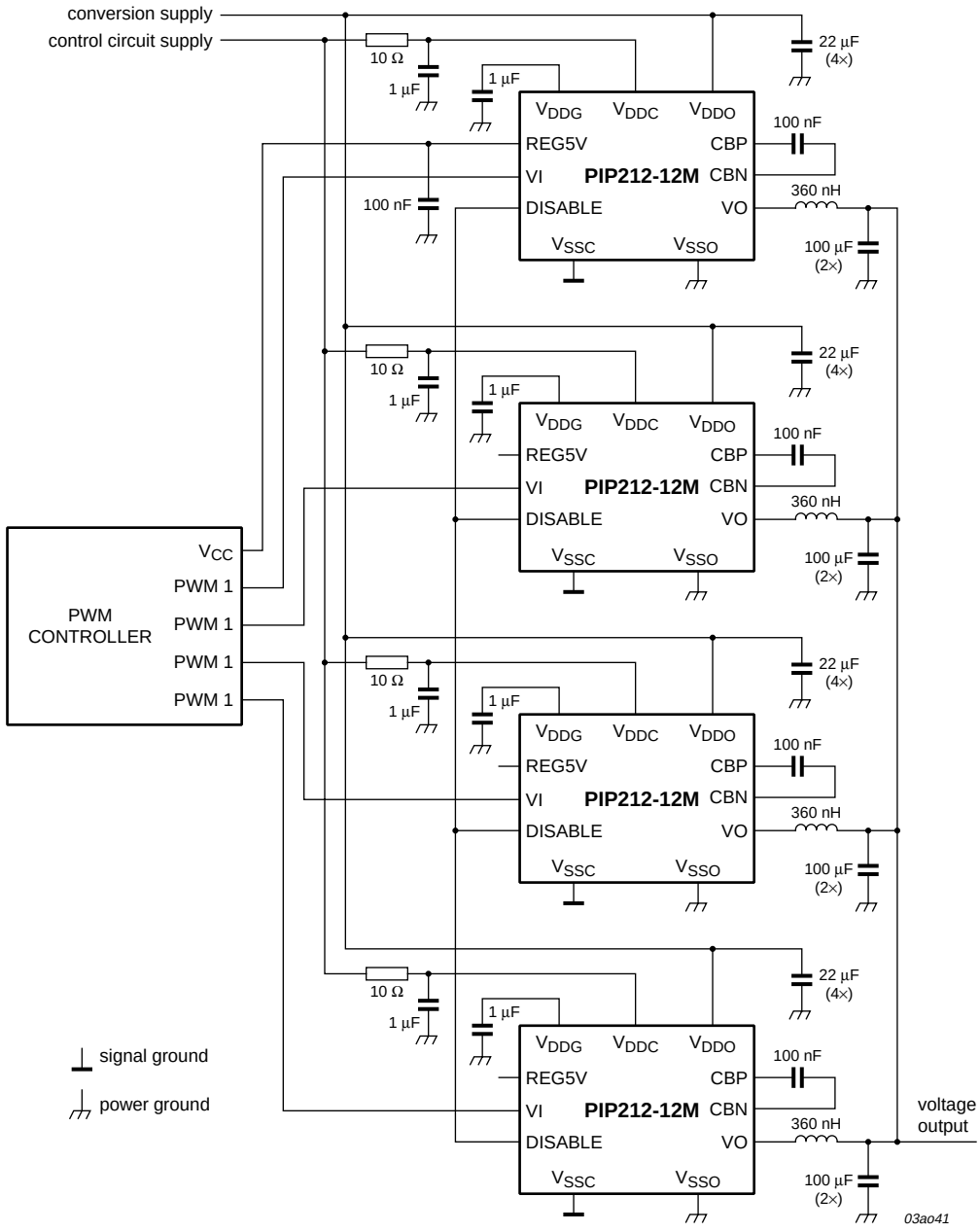



**Fig 10. Typical application circuit using the PIP212-12M in a four-phase converter**

A typical four-phase buck converter is shown in Figure 10. This system uses four PIP212-12M devices to deliver a continuous output current of 120 A at an operating frequency of 500 kHz.



© NXP B.V. 2006. All rights reserved.

## 12.2 $V_{DDG}$ supply options

The following options can be used for the lower MOSFET driver supply ($V_{DDG}$).

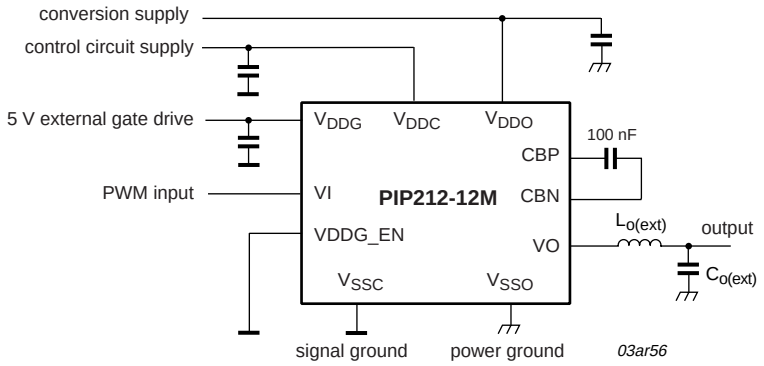



**Fig 11. Dual supply operation using 5 V external supply for $V_{DDG}$**

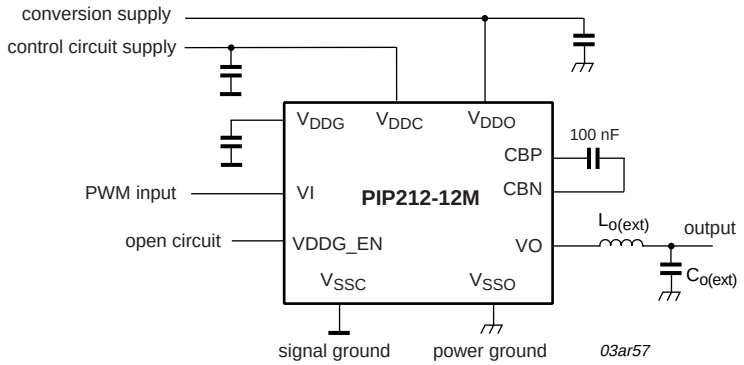



**Fig 12. Single supply operation using internal supply for $V_{DDG}$**

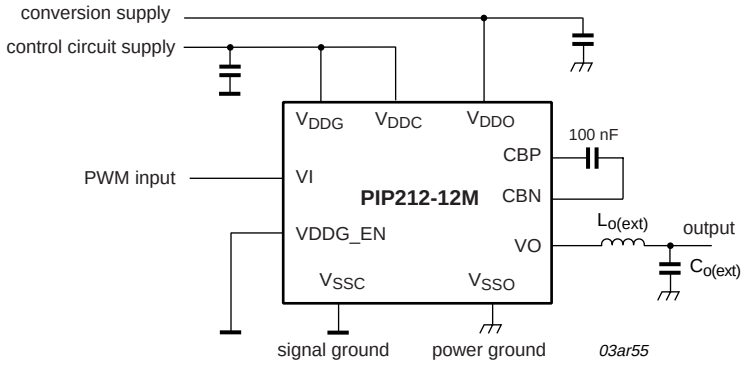



**Fig 13. Single supply operation using external supply for $V_{DDG}$**

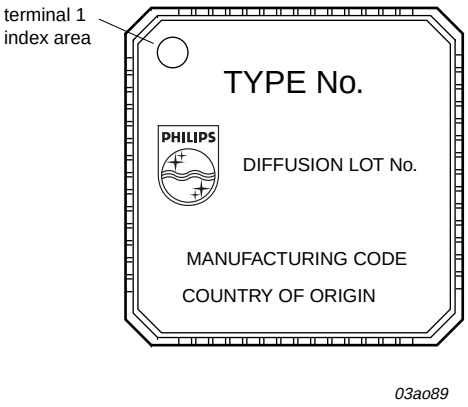


© NXP B.V. 2006. All rights reserved.

### 12.3 DrMOS compatibility

The PIP212-12M can be configured to be compatible with the Intel DrMOS specification. Conformance to the Intel DrMOS specification requires that an external power supply to the $V_{DDG}$ pin is used and hence the internal $V_{DDG}$ regulator must be disabled by connecting the VDDG_EN pin to $V_{SSC}$. The PRDY flag is not used and should be left unconnected on the PCB. The external boost capacitor should also be connected between CBP and $V_O$ and not CBP and CBN with the CBN pin being left unconnected on the PCB. In addition, $V_{SSC}$ pin 7 and $V_{SSO}$ pin 39 to pin 41 should be left unconnected on the PCB. Note that the sizes of PAD 1, PAD 2 and PAD 3 can vary between different DrMOS vendors. The PCB footprint must be modified to take the pinning modifications and pad size differences into account. To ensure footprint compatibility with other DrMOS products, it is recommended that the latest multiple vendor compatibility PCB footprint contained within the Intel DrMOS specification is used and that the relevant DrMOS product data sheet is checked for compatibility.

## 13. Marking




TYPE No: PIP212-12M_NN (NN is revision number)

DIFFUSION LOT No: 7 characters

MANUFACTURING CODE; see Figure 15

COUNTRY OF ORIGIN: Korea

**Fig 14. SOT684-4 marking**

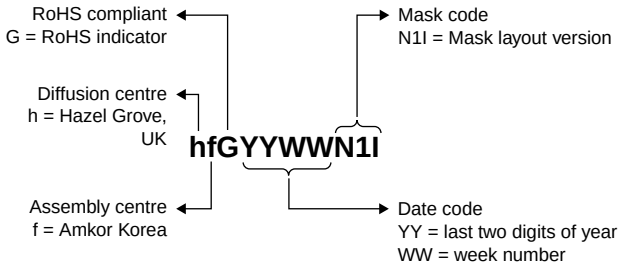


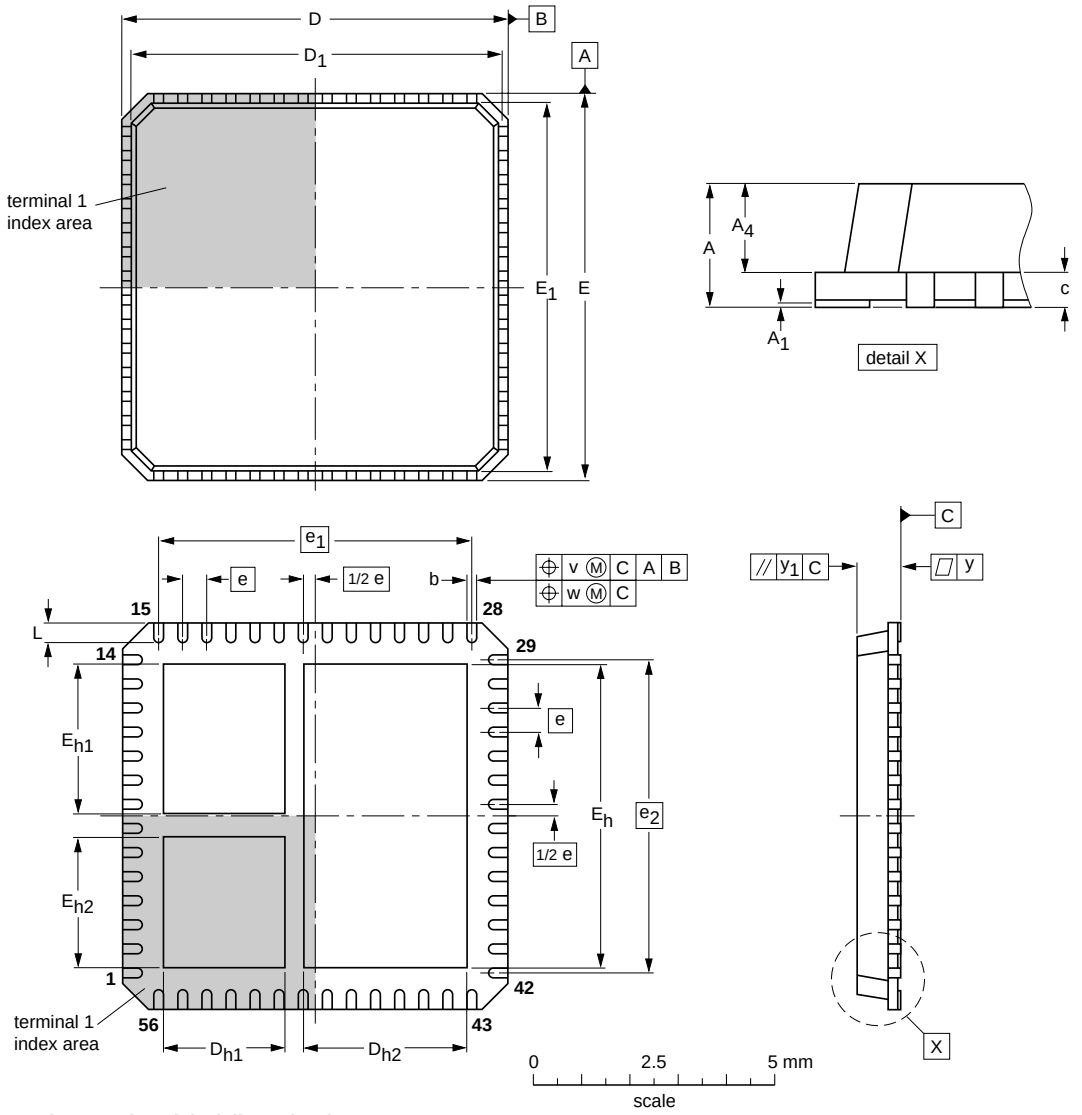

**Fig 15. Interpretation of manufacturing code**



© NXP B.V. 2006. All rights reserved.

## 14. Package outline

**HVQFN56: plastic thermal enhanced very thin quad flat package; no leads; 56 terminals; body 8 x 8 x 0.85 mm** **SOT684-4**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_4$ | b | c | D | $D_1$ | $D_{h1}$ | $D_{h2}$ | E | $E_1$ | $E_h$ | $E_{h1}$ | $E_{h2}$ | e | $e_1$ | $e_2$ | L | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 0.9 | 0.05<br>0.00 | 0.70<br>0.65 | 0.30<br>0.18 | 0.2 | 8.1<br>7.9 | 7.8<br>7.7 | 2.65<br>2.35 | 3.55<br>3.25 | 8.1<br>7.9 | 7.8<br>7.7 | 6.45<br>6.15 | 3.25<br>2.95 | 2.85<br>2.55 | 0.5 | 6.5 | 6.5 | 0.5<br>0.3 | 0.1 | 0.05 | 0.05 | 0.1 |

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT684-4 | - - - | MO-220 | - - - | | | ~~03-10-23~~<br>04-09-14 |

**Fig 16. Package outline SOT684-4 (HVQFN56)**


© NXP B.V. 2006. All rights reserved.

# 15. Soldering

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

## 15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

## 15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus PbSn soldering

## 15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities



© NXP B.V. 2006. All rights reserved.

## 15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 17) than a PbSn process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 7 and 8

**Table 7. SnPb eutectic process (from J-STD-020C)**

| Package thickness (mm) | Package reflow temperature (°C) | |
|---|---|---|
| | Volume ($mm^3$) | |
| | < 350 | ≥ 350 |
| < 2.5 | 235 | 220 |
| ≥ 2.5 | 220 | 220 |

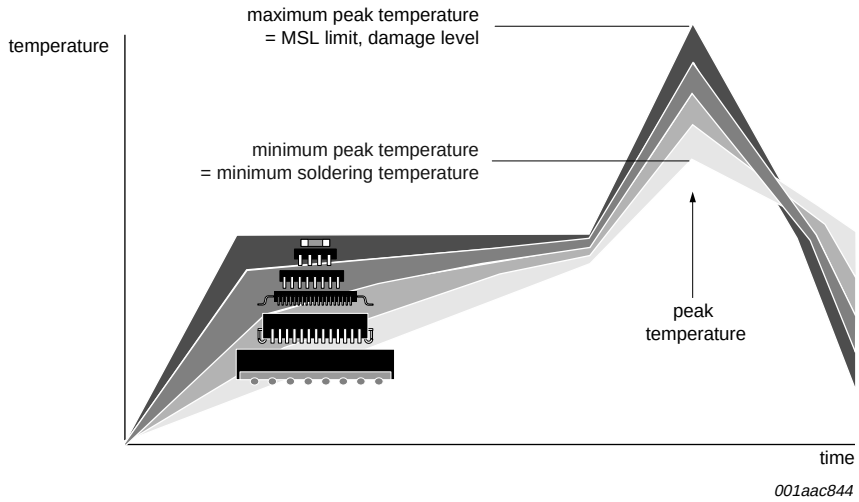
**Table 8. Lead-free process (from J-STD-020C)**

| Package thickness (mm) | Package reflow temperature (°C) | | |
|---|---|---|---|
| | Volume ($mm^3$) | | |
| | < 350 | 350 to 2000 | > 2000 |
| < 1.6 | 260 | 260 | 260 |
| 1.6 to 2.5 | 260 | 250 | 245 |
| > 2.5 | 250 | 245 | 245 |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 17.


© NXP B.V. 2006. All rights reserved.




MSL: Moisture Sensitivity Level

**Fig 17. Temperature profiles for large and small components**

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

# 16. Mounting

## 16.1 PCB design guidelines

The terminals on the underside of the package are rectangular in shape with a rounded edge on the inside. Electrical connection between the package and the printed-circuit board is made by printing solder paste onto the PCB footprint followed by component placement and reflow soldering. The PCB footprint shown in Figure 18 is designed to form reliable solder joints.

The use of solder resist between each solder land is recommended. PCB tracks should not be routed through the corner areas shown in Figure 18. This is because there is a small, exposed remnant of the leadframe in each corner of the package, left over from the cropping process.

Good surface flatness of the PCB lands is desirable to ensure accuracy of placement after soldering. Printed-circuit boards that are finished with a roller tin process tend to leave small lumps of tin in the corners of each land. Levelling with a hot air knife improves flatness. Alternatively, an electro-less silver or silver immersion process produces completely flat PCB lands.


© NXP B.V. 2006. All rights reserved.

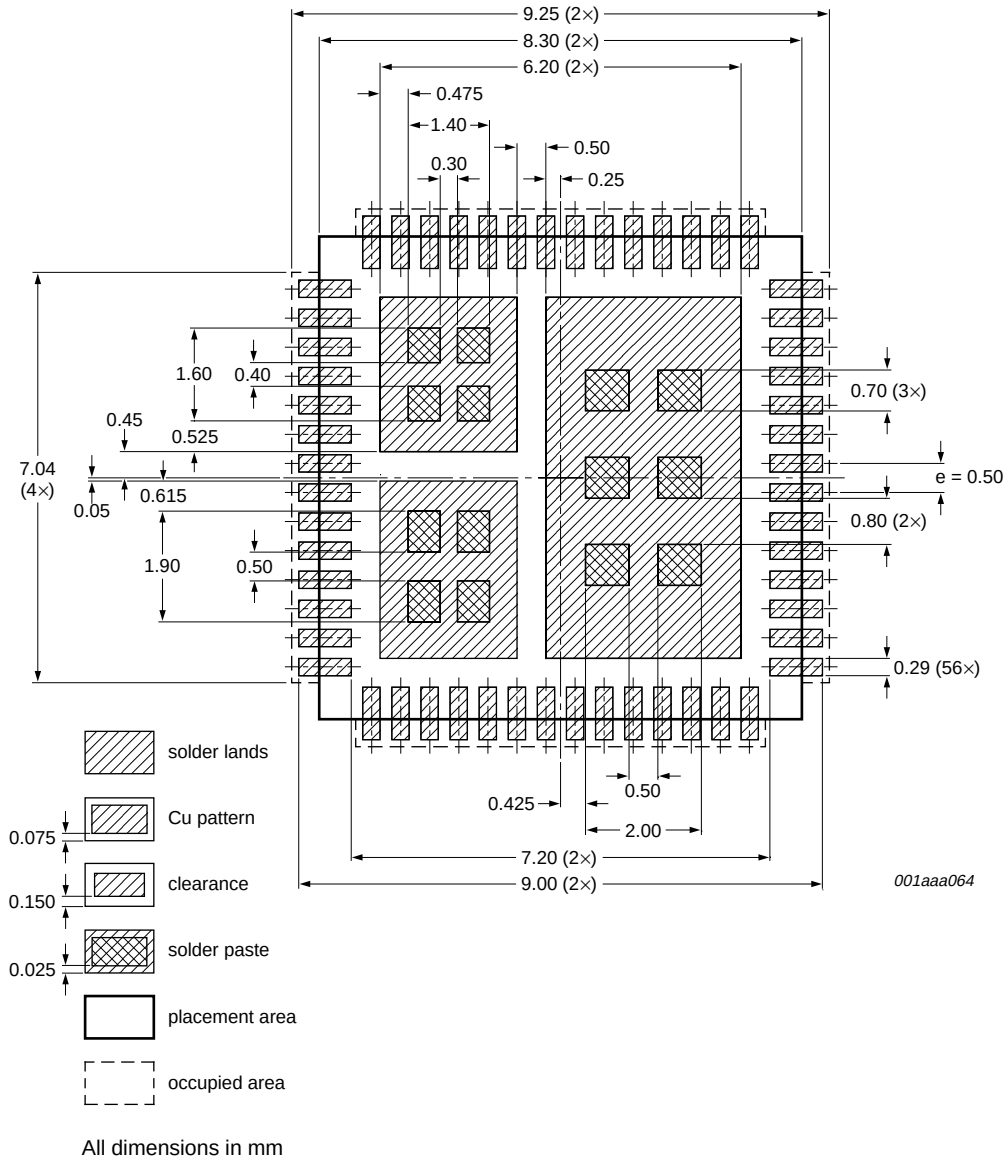



**Fig 18. PCB footprint for SOT684-4 package (reflow soldering)**

## 16.2 Solder paste printing

The process of printing the solder paste requires care because of the fine pitch and small size of the solder lands. A stencil thickness of 0.125 mm is recommended. The stencil apertures can be made the same size as the solder lands in Figure 18.

The type of solder paste recommended for MLF (Micro Lead-Frame) packages is “No clean”, Type 3, due to the difficulty of cleaning flux residues from beneath the MLF package.



© NXP B.V. 2006. All rights reserved.

## 17. Revision history

**Table 9. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| PIP212-12M_4 | 20061023 | Product data sheet | ECN 211443 | PIP212-12M_3 |
| Modifications: | • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.<br>• Legal texts have been adapted to the new company name where appropriate. | | | |
| PIP212-12M_3 | 20060803 | Product data sheet | - | PIP212-12M_2 |
| PIP212-12M_2 (9397 750 14586) | 20050302 | Preliminary data sheet | - | PIP212-12M_1 |
| PIP212-12M_1 (9397 750 14464) | 20041223 | Objective data sheet | - | - |


© NXP B.V. 2006. All rights reserved.

# 18. Legal information

## 18.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

## 18.2 Definitions

**Draft —** The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet —** A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

## 18.3 Disclaimers

**General —** Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

**Right to make changes —** NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use —** NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of a NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications —** Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

**Limiting values —** Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Terms and conditions of sale —** NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

**No offer to sell or license —** Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

## 18.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

# 19. Contact information

For additional information, please visit: **http://www.nxp.com**

For sales office addresses, send an email to: **salesaddresses@nxp.com**



© NXP B.V. 2006. All rights reserved.

## 20. Contents


**1 General description . . . . . 1**
**2 Features . . . . . 1**
**3 Applications . . . . . 1**
**4 Ordering information . . . . . 2**
**5 Block diagram . . . . . 2**
**6 Functional diagram . . . . . 3**
**7 Pinning information . . . . . 3**
7.1 Pinning . . . . . 3
7.2 Pin description . . . . . 4
**8 Functional description . . . . . 4**
8.1 Basic operation . . . . . 4
8.2 UnderVoltage Lockout (UVLO) . . . . . 4
8.3 Upper driver operation . . . . . 5
8.4 $V_{DDG}$ regulator . . . . . 5
8.5 3-state function . . . . . 5
8.6 Automatic Dead-time Reduction (ADR) . . . . . 5
8.7 Over Temperature Protection (OTP) . . . . . 6
8.8 Disable . . . . . 6
8.9 Reg5V . . . . . 6
**9 Limiting values . . . . . 7**
**10 Thermal characteristics . . . . . 7**
**11 Characteristics . . . . . 8**
**12 Application information . . . . . 11**
12.1 Typical application . . . . . 11
12.2 $V_{DDG}$ supply options . . . . . 12
12.3 DrMOS compatibility . . . . . 13
**13 Marking . . . . . 13**
**14 Package outline . . . . . 14**
**15 Soldering . . . . . 15**
15.1 Introduction to soldering . . . . . 15
15.2 Wave and reflow soldering . . . . . 15
15.3 Wave soldering . . . . . 15
15.4 Reflow soldering . . . . . 16
**16 Mounting . . . . . 17**
16.1 PCB design guidelines . . . . . 17
16.2 Solder paste printing . . . . . 18
**17 Revision history . . . . . 19**
**18 Legal information . . . . . 20**
18.1 Data sheet status . . . . . 20
18.2 Definitions . . . . . 20
18.3 Disclaimers . . . . . 20
18.4 Trademarks . . . . . 20
**19 Contact information . . . . . 20**
**20 Contents . . . . . 21**


Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

**© NXP B.V. 2006.** **All rights reserved.**

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

**Date of release: 23 October 2006**
**Document identifier: PIP212-12M_4**

founded by

PHILIPS